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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,144	HOYLE ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/00 and 2/6/01 and 2/14/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration (resubmitted) as received on 2/14/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 9 is objected to because of the following informalities:

   a. Lines 3-5 of claim 9 recite the limitation "CPU." This term lacks antecedent basis. Please correct to read "microprocessor" as the previous claim language has provided antecedent basis for.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Black et al., U.S. Patent No. 5,761,723.

7. Regarding claim 1, Black has taught a digital system comprising a microprocessor (10 of Fig.1) having an instruction execution pipeline with a plurality of pipeline phases (see Col.4 lines 49-54, Col.6 lines 8-11 and Fig.2), wherein the microprocessor comprises:

a. Program fetch circuitry (see Col.3 lines 9-11, Col.4 lines 61-67, Col.5 lines 1-5, and 46/48/60 of Fig.3) operable to perform a first portion of the plurality of pipeline phases (see Fig.2);

b. Instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry (see Col. 5 lines 6-15 and 52/54/56 of Fig.3), the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases (see Fig.2);

c. At least a first functional unit (20 of Fig.1) connected to receive a plurality of control signals from the instruction decode circuitry (see Figs.1 and 3), the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases (see Fig.2 and Col.5 lines 30-38), wherein the first functional unit comprises:

i. First test circuitry connected to receive an operand from a selected test register (37 of Fig.1), and having an output for indicating a condition of the operand (see Col.9 lines 28-34 and Col.10 lines 22-23);

ii. Decrement circuitry connected to receive the operand from the selected test register (37 of Fig.1), and having an output connected to provide a decremented value of the operand to the test register (see Col.10 lines 62-65);

iii. Adder circuitry connected to receive a program counter value and a displacement value, and having an output connected to conditionally provide a branch address to a program counter register (see Col.9 lines 47-65 and Col.10 lines 56-59);

iv. Wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the operand, decrement the operand, and conditionally provide a branch address to the program counter in response to a single instruction of a first type (see Col.9 lines 19-25, Col.10 lines 62-65, and Col.11 lines 25-30 and 57-59).

8. Regarding claim 2, Black has taught the digital system of claim 1, wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the operand, and conditionally provide a branch address to the program counter in response to a single instruction during a single one of the third portion of pipeline phases (see Col.8 lines 28-37).

9. Regarding claim 3, Black has taught the digital system of claim 1, wherein the first test circuitry is operable to inhibit the program counter from receiving the branch address if the operand has a value that does not correspond to a first condition (see Col.10 lines 56-62). By deleting the calculated branch address from the branch target address cache prior to the completion of the instruction in response to a value in the counter register (37 of Fig.1), one is inhibiting the program counter from receiving the branch target address.

10. Regarding claim 4, Black has taught the digital system of claim 3, further comprising second test circuitry connected to test a condition of a selected predicate register (39 of Fig.1), and having an output for indicating a condition of the predicate register, wherein the second test circuitry is operable to inhibit the program counter from receiving the branch address if the contents of the predicate register do not correspond to a second condition (see Col.9 lines 28-46 and Col.10 lines 22-23). By deleting the calculated branch address from the branch target address cache prior to the completion of the instruction in response to a value in the condition register (39 of Fig.1), one is inhibiting the program counter from receiving the branch target address (see Col.10 lines 41-43).

11. Regarding claim 5, Black has taught the digital system of claim 4, wherein the program counter is operable to receive the branch address from the adder circuitry only when the contents of the test register correspond to the first condition and the contents of the predicate register correspond to the second condition (see Col.9 lines 26-34). When a branch is resolved as not taken, the program counter will not receive an address from the adder circuitry which reflects a branch address, but will continue fetching from the current program counter address.

12. Regarding claim 10, Black has taught a method of operating a digital system having a microprocessor (10 of Fig.1) with a conditional branch instruction (Col.9 lines 8-25), comprising the steps of:

a. Fetching a conditional branch instruction for execution (see Col.4 lines 55-67 and Fig.2);

b. Testing a test register (37 of Fig.1) selected by the conditional branch instruction to determine if the contents of the test register meet a first condition (see Col.9 lines 35-45);

c. Providing a branch address to a program counter to cause a branch if the contents of the test register (37 of Fig.1) meet the first condition (see Col.8 lines 27-37 and Col.9 lines 28-34);

d. Modifying the contents of the test register (see Col.10 lines 62-65).

13. Regarding claim 11, Black has taught the method of claim 10, further comprising the steps of:

a. Testing a predicate register (39 of Fig.1) selected by the conditional branch instruction to determine if the contents of the predicate register meet a second condition (see Col.9 lines 10-16 and Col.10 lines 22-24). Conditional branch instructions are decoded by the instruction decoder (56 of Fig.3) during the decode stage of the pipeline (see Fig.2) in order to determine what the branch conditions are, as well as which register, the test or predicate, is to be tested;

b. Inhibiting the step of providing a branch address to the program counter if the contents of the predicate register (39 of Fig.1) do not meet the second condition (see Col.9 lines 28-46 and Col.10 lines 22-23). By deleting the calculated branch address from the branch target address cache prior to the completion of the instruction in response to a value in the condition register (39 of Fig.1), one is inhibiting the program counter from receiving the branch target address (see Col.10 lines 41-43).

14. Regarding claim 12, Black has taught the method of claim 10 as shown above, wherein the step of modifying decrements the test register (37 of Fig.1) (see Col.10 lines 62-65).

15. Regarding claim 13, Black has taught the method of claim 10 as shown above, wherein the steps of testing, providing, and modifying are all performed during a same execution phase of the microprocessor. While not taught explicitly, it is inherent that the steps of testing, providing, and modifying all are all performed during the execution phase of the microprocessor because the steps all take place within the branch unit (20 of Fig.1), which is an execution unit that operates only during the execution phase of the pipeline (see Col.5 lines 30-38, Col.8 lines 28-37 and Col.10 lines 62-65).

16. Regarding claim 14, Black has taught the method of claim 10 as shown above, wherein the step of modifying is inhibited if the contents of the test register do not meet the first condition (see Col.8 lines 28-33 and Col.10 lines 62-65). While not taught explicitly, it is inherent that when the condition to branch is not met by the contents of the test register, the count in the test register is already at zero and thus an instruction that branches on a non-zero value in the test register is not supposed to branch (see Col.10 lines 44-52), and the count cannot be decremented any further.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Black et al., U.S. Patent No. 5,761,723, in further view of the *PowerPC Microprocessor Family: The Programming Environments*.

19. Regarding claim 6, Black has taught the digital system of claim 1 as shown above, wherein the instruction of a first type identifies the test register and a displacement value to determine the fetch address (see Col.9 lines 26-34). Black has not explicitly taught a specific instruction format containing a field for identifying the test register and a field to provide a displacement value.

20. However, the *PowerPC Microprocessor Family: The Programming Environments* has taught a "branch conditional" instruction (see p.8-24), which contains a field for identifying the test register (see "BO = 0101y" on p.8-24) and a field to provide a displacement value (see "target_addr" and "BD" on p.8-24, as well as "AA = 0" section on p.8-25). Black has taught an exemplary embodiment of his microprocessor implementing the PowerPC architecture (see Col.9 lines 9-11). One of ordinary skill in the art would have found it obvious to implement PowerPC instructions on a microprocessor that utilizes the PowerPC instruction set to execute conditional branch instructions that contain fields for identifying a test register and provide a displacement value.

21. Regarding claim 7, Black has taught the digital system of claim 6 as shown above, wherein the instruction of a first type identifies the predicate register (see Col.9 lines 26-34). Black has not explicitly taught a specific instruction format containing a field for identifying the predicate register.

22. However, the *PowerPC Microprocessor Family: The Programming Environments* has taught a "branch conditional" instruction (see p.8-24), which contains a field for identifying the predicate register (see "BI" field and its description on p.8-24). Black has taught an exemplary embodiment of his microprocessor implementing the PowerPC architecture (see Col.9 lines 9-11). One of ordinary skill in the art would have found it obvious to implement PowerPC instructions on a microprocessor that utilizes the PowerPC instruction set to execute conditional branch instructions that contain fields for identifying a predicate register.

23. Regarding claim 8, Black has taught a test register (37 of Fig.1) and a predicate register (39 of Fig.1) both residing within the same functional unit (20 of Fig.1). Black has not explicitly taught the test and predicate registers being located in the same register file.

24. However, one of ordinary skill in the art would have recognized that registers that are commonly used are usually grouped together to exploit spatial and temporal locality. Black has taught a separate group of general purpose registers (32 of Fig.1) which do not contain the test and predicate registers. Because the test and predicate registers are not located in the general purpose register file, but in the branch unit, one of ordinary skill in the art at the time of the invention would have found it obvious to include these two commonly used registers in the same register file within the branch unit (20 of Fig.1) so as to allow the hardware to exploit spatial and temporal locality.

25. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Black et al., U.S. Patent No. 5,761,723 as applied to claim 1 above, and further in view of Willkie et al., U.S. Patent No. 5,923,705.

26. Regarding claim 9, Black has taught the digital system of claim 1, but has not taught the digital system being a cellular telephone. Willkie has taught a cellular telephone (14 of Fig.1) comprising:

a. An integrated keyboard connected to the CPU via a keyboard adapter (see Fig.1);

b. A display, connected to the CPU via display adapter (see Fig.1);

c. Radio frequency circuitry connected to the CPU (see Fig.2);

d. An aerial connected to the RF circuitry (see Fig.1).

27. One of ordinary skill in the art would have recognized that modern cellular phones require a processor to process digital data and voice signals that are received and transmitted from the phones (see Willkie Col.1 lines 15-20 and 28-31). Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to use the processor (10 of Black Fig.1) in a cellular telephone digital system to process digital data and voice signals.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

29. McGarity, U.S. Patent No. 5,687,349, has taught a processor embodying the PowerPC architecture with specialized branch instructions and branch prediction hardware.

30. Miyake et al., U.S. Patent No. 6,047,371, has taught a digital signal processor with specialized hardware to process conditional branch instructions more efficiently.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO

9/11/03

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